

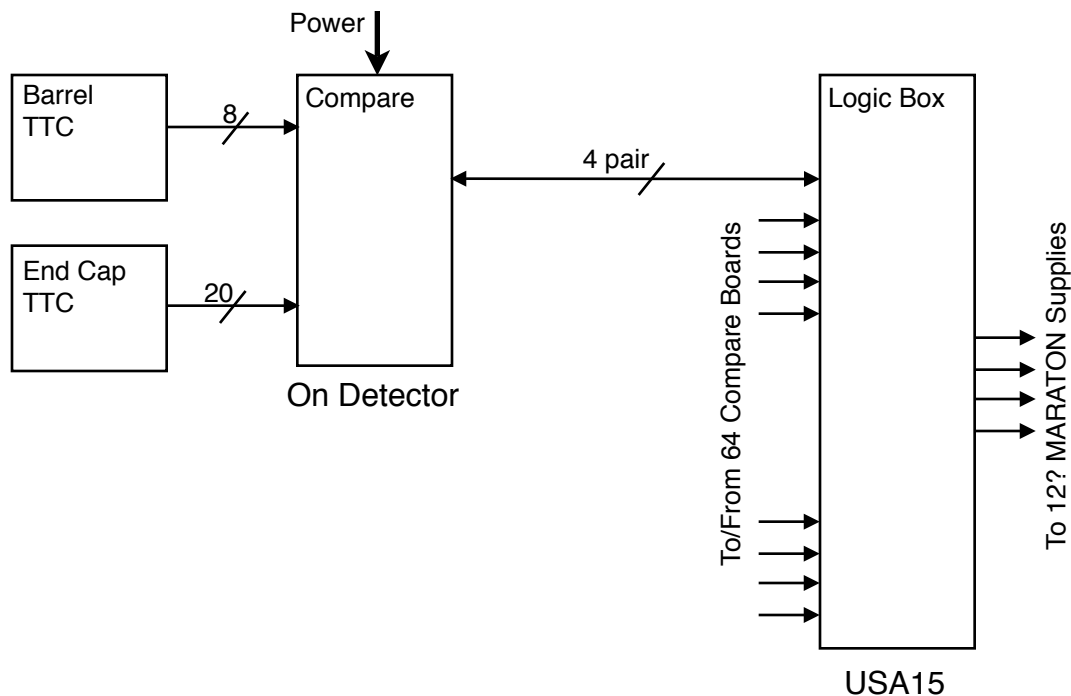
Proposal for a hardware interlock based on TRT electronics temperature

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System Architecture



The ATLAS TRT barrel and end cap readout boards include a NTC (negative temperature coefficient) thermistor. These are accessible from a connector on the recently re-designed TTC PP (patch panel) boards.

We propose an interlock system based on two types of modules:

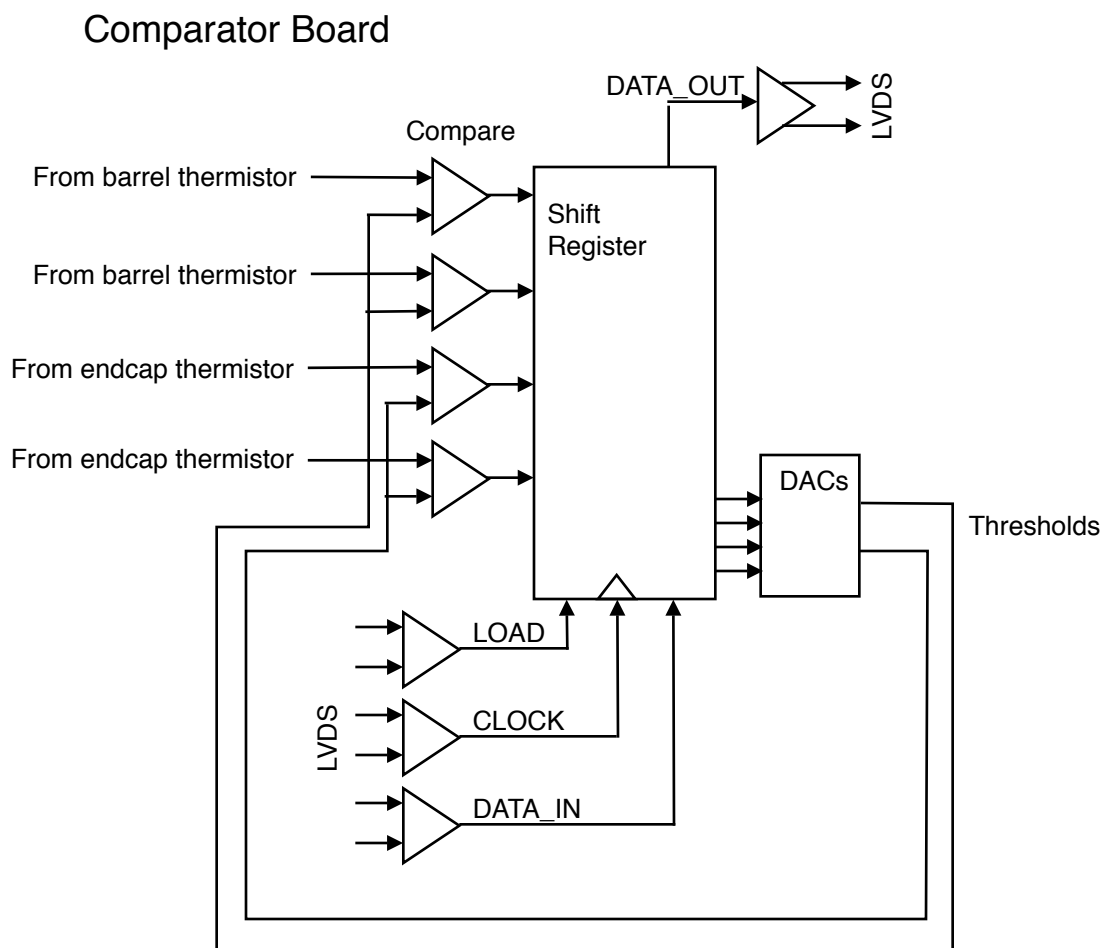
- 1) A “comparator” board which mounts on or near the patch panel boxes and has a comparator and a shift register bit per thermistor. This would handle 1 PP2 box which includes 1 Barrel and 1 End Cap TTC board. The thermistor signals connect via short ERNI 26 wire cables.
- 2) A “logic” box which drives and receives the comparator/shift boards, implements the “Alarm” logic, and shuts down the supplies if necessary. This would be rack mounted in the USA15 area.

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The two types of boards will be connected by digital, differential (LVDS) signaling over “ethernet” twisted pair cables. Four pairs are required:

Clock
Load
Data In
Data Out

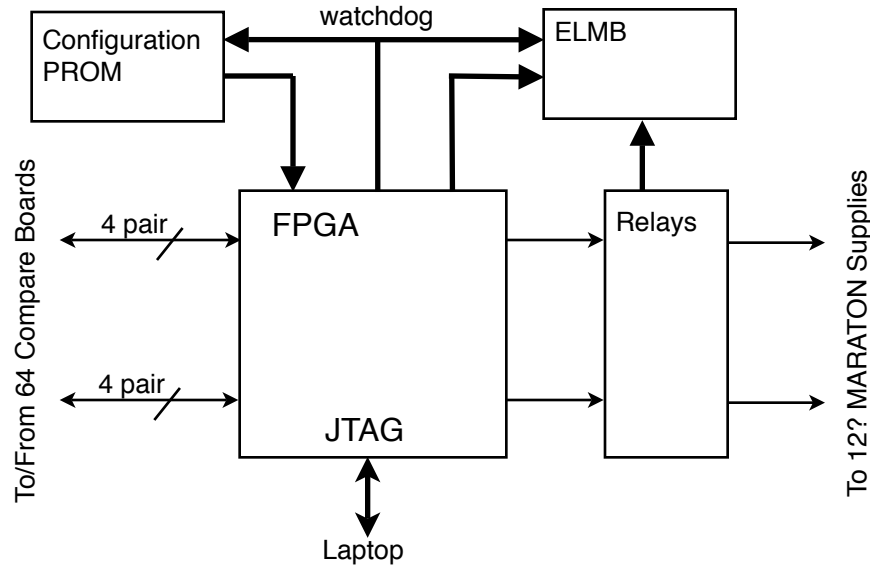
This allows us to check the data path by shifting in known data and verifying that the same data comes back. Two DACs set the comparator thresholds for the two sets of thermistors.



We propose running 64 new “ethernet” cables from the USA15 area to each of the PP2 boxes.

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Logic Board



For mapping out the thermistor “addresses”, checking the cabling, optimizing the thresholds, etc, special FPGA configurations can be loaded through the JTAG port. Logic (e.g. Xilinx “Chipscope”) can be included in the FPGA configuration to output information through the JTAG port for debugging. Once everything is working, the final FPGA configuration will be loaded from a PROM.

The FPGA logic will include “watch-dog” logic which reloads the FPGA from the PROM in case the logic becomes corrupted.

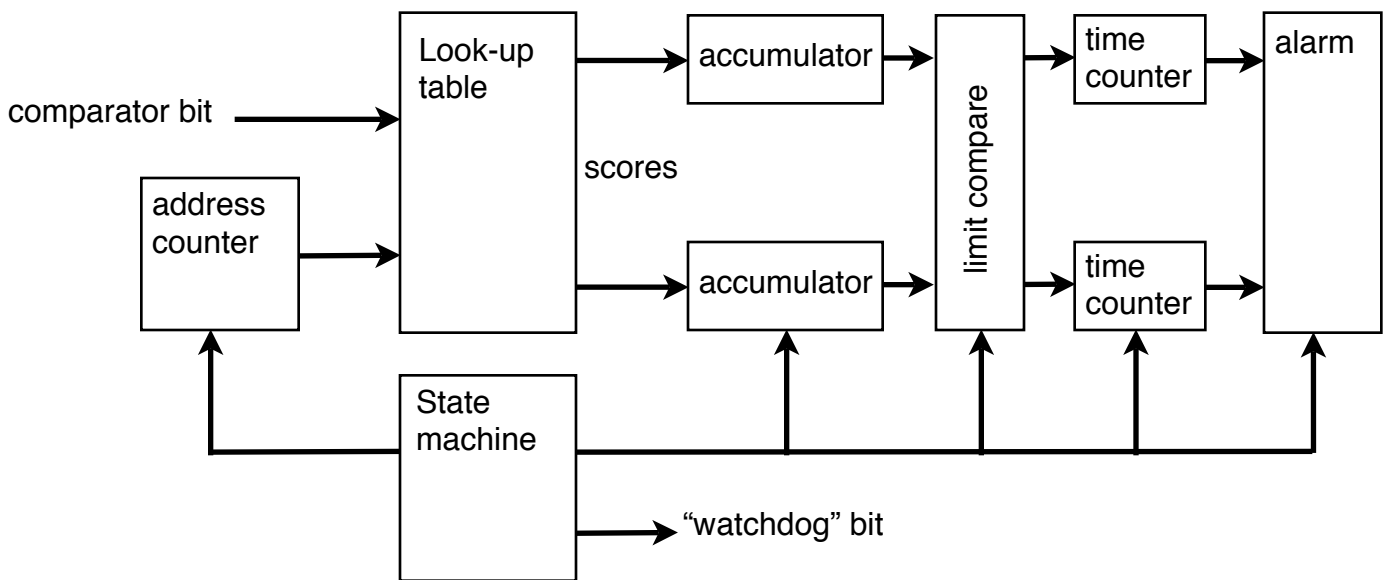
The status of the logic board can be monitored by the Detector Control System through an ELMB board.

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The algorithm for the FPGA logic could be:

Generate an address for each thermistor bit by counting the number of clock pulses driving the shift registers. Use this address as the input to a look-up table which maps to the appropriate MARATON supply and assign a “score” if the thermistor compare bit is on. For example, some thermistors may not work; the look-up table could be programmed to ignore these channels. It may be desirable to weight the endcap thermistors differently from the barrel thermistors. Accumulate this “scoring” of thermistors. If the accumulated “score” exceeds a limit for some time “alarm” and shut down the appropriate bulk power supply.

FPGA algorithm



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General questions:

Where should power be cut?

- at the AC distribution in USA15?
- at the MARATON supply interlock?

What level of DCS monitoring/control is needed? What information does the ELMB board see?

Specific questions:

How and where should the compare boards be mounted? Should it attach to the PP2 box? How long should the 26 wire ERNI cables be from the TTC boards to the compare board? How long should the compare board power wires be?

Does the alarm logic (in USA15) also need to be rad-tolerant? We are assuming no. Is an FPGA suitable? Does this logic need to be monitored or controlled by the DCS system, and if so, what parameters?

What is the optimum "Alarm" logic? To allow for some flexibility, we propose implementing this logic in an FPGA.

How difficult will it be to run cables from USA15 to the MARATON supplies if we choose to cut power there? If cutting the AC primary power is preferred, how is this accomplished?